AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1-22. (Cancelled)

23. (Currently Amended) A computer system according to claim ~~21~~30,

wherein said first main memory has a region for a first page structure of said first main memory and

has a region for a second page structure of said second main memory, and

wherein said processor accesses said first main memory using said first page structure.

24. (Currently Amended) A computer system according to claim ~~21~~30,

wherein said non-volatile storage is EEPROM.

25. (Currently Amended) A computer system according to claim ~~21~~30, further comprising:

a connecting switch connecting said processor, said first main memory and said non-volatile storage.

26. (Currently Amended) A computer system supporting a virtual memory system, said computer system comprising,

a processor,

a first main memory which said processor accesses,

a non-volatile storage storing first memory size information regarding said first main memory and second memory size ~~configuration~~ information regarding a second main memory to be hot plugged, and

a housing including said processor, said first main memory and said non-volatile storage,

wherein said processor has an address translating unit translating virtual addresses and physical addresses,

said processor outputs physical addresses representing a region of said first main memory,

wherein said first main memory has at least a part of address translation information of said first main memory and has a first region in which address translation information for said second main memory is to be stored,

wherein said processor has a unit translating logical-physical addresses, accesses said address translation information for said first main memory and generates physical addresses, and

wherein said first main memory stores said address translation information for said first main memory in a top priority region of interrupt handling and assigns said first region in said top priority region.

27-29. (Cancelled)

30. (Previously Presented) A computer system, comprising:

a processor generating an address of a virtual address system,

a first main memory storing information which said processor processes, and

a non-volatile storage storing first memory size information of said first main memory and second memory size information of a second main memory that is to be hot-added, and a case housing said processor, said first main memory, and said non-volatile storage,

wherein said processor has an address translating unit translating virtual addresses and physical addresses,

said processor outputs physical addresses representing a region of said first main memory,

wherein said first main memory has at least a part of address translation information of said first main memory and has a first region in which address translation information for said second main memory is to be stored,

wherein said processor has a unit translating logical-physical addresses, accesses said address translation information for said first main memory and generates physical addresses, and

wherein said first main memory stores said address translation information for said first main memory in a top priority region of interrupt handling and assigns said first region in said top priority region.

31. (Currently Amended) A computer system according to claim ~~29~~30, further comprising a connecting switch connecting said processor and said first main memory.

32. (Currently Amended) A computer system comprising,

a first main memory,

a processor processing information stored in said first main memory,

a non-volatile storage storing first memory size information of said first main memory and second memory size ~~memory~~ information of a second main memory to be hot-inserted while said computer system is powered, and

a housing including said first main memory, said processor, and said non-volatile storage,

wherein said processor has an address translating unit translating virtual addresses and physical addresses,

said processor outputs physical addresses representing a region of said first main memory,

wherein said first main memory has at least a part of address translation information of said first main memory and has a first region in which address translation information for said second main memory is to be stored,

wherein said processor has a unit translating logical-physical addresses, accesses said address translation information for said first main memory and generates physical addresses, and

wherein said first main memory stores said address translation information for said first main memory in a top priority region of interrupt handling and assigns said first region in said top priority region.

33-34. (Cancelled)

35. (Previously Presented) A computer system according to claim 32,

wherein said first main memory has at least part of first logical-physical address translating pairs of said first main memory and has an assigned region to store second logical-physical address translating pairs of said second main memory, and

wherein said first logical-physical address translating pairs are used for said processor accessing said first main memory.

36. (Previously Presented) A computer system according to claim 35,

wherein said processor has a logical-physical address translating unit and said logical-physical address translating unit uses said first logical-physical address translating pairs when said processor accesses said first main memory.

37. (Previously Presented) A computer system according to claim 35,

wherein said first main memory has an untranslatable region and stores said first logical-physical address translating pairs in said untranslatable region.

38. (Previously Presented) A computer system according to claim 37,

wherein said first main memory has an untranslatable region and stores said first logical-physical address translating pairs in said untranslatable region.

39. (Previously Presented) A computer system according to claim 32, wherein said non-volatile storage is EEPROM.

40. (Previously Presented) A computer system according to claim 32, further comprising a connecting switch connecting said processor and said first main memory.

41. (Currently Amended) A computer system, allowing a main memory to be hot-added while said computer system is powered on, comprising,

a first main memory,

a processor accessing said first main memory with a virtual memory system,

a non-volatile storage storing first memory information of said first main memory and second memory size information of a second main memory to be hot-added while powered on, and

a body housing said first main memory, said processor and said non-volatile storage,

wherein said processor has an address translating unit translating virtual addresses and physical addresses,

said processor outputs physical addresses representing a region of said first main memory,

wherein said first main memory has at least a part of address translation information of said first main memory and has a first region in which address translation information for said second main memory is to be stored,

wherein said processor has a unit translating logical-physical addresses, accesses said address translation information for said first main memory and generates physical addresses, and

wherein said first main memory stores said address translation information for said first main memory in a top priority region of interrupt handling and assigns said first region in said top priority region.

42. (Previously Presented) A computer system according to claim 41,

wherein said non-volatile storage is EEPROM.

43. (Previously Presented) A computer system according to claim 41, further comprising a connecting switch connecting said processor and said first main memory.

44. (Previously Presented) A computer system according to claim 41,

wherein said first main memory has a first logical-physical address translating table for said first main memory, and

further has a region to store a second logical-physical address translating table for said main memory to be hot added.

45. (Previously Presented) A computer system according to claim 41,

wherein said first main memory has an untranslatable region and stores said first logical-physical address translating table in said untranslatable region.

46. (Previously Presented) A computer system according to claim 41,

wherein said first main memory further assigns said region to store a second logical-physical address translating table for said main memory to be hot-added in said untranslatable region.